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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/727,744	12/01/2000	Lawrence Richard Fontaine	RA 5312 (1028.1132101)	4178

7590 10/22/2003

Charles A. Johnson
UNISYS Corporation
P O Box 64942
M.S. 4773
St. Paul, MN 55164

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/727,744	FONTAINE ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2000 and 26 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-27 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Corrected Paper as received on 02 April 2001 and IDS as received on 26 April 2001.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "158" in Figure 7 has been used to designate both the connection between the memory interface and instruction cache tag logic and the connection between I-FLC and instruction read address control. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Page 12, lines 14 and 21, element number "30" and Page 12, line 20, element number "32". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 7, elements 158, 158b, 192, 175, and 309. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office

action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

7. Claims 11-18 and 20-26 are objected to because of the following informalities: The claims were originally misnumbered by having two claims labeled "2". The office has renumbered the claims. However, the dependencies on claims 11-18 and 20-26 are incorrect. Please correct the claims dependencies, i.e. claims 11-18 are now dependent on claim 10 instead of claim 9 and claims 20-26 are now dependent on claim 19 instead of claims 18. Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-18 rejected under 35 U.S.C. 102(b) as being taught by Nakayama et al., U.S. Patent Number 4,788,655 (herein referred to as Nakayama).

10. Referring to claim 1, Nakayama has taught a method for storing a digital value to memory in a pipelined instruction processor, wherein the digital value is read from memory in response to a conditional jump instruction to determine if the condition of the conditional jump

instruction is satisfied (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B), the method comprising:

a. Generating at least one status bit based on the digital value to be stored, the at least one status bit indicating if a predetermined condition of a conditional jump instruction is satisfied (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B); and

b. Storing the digital value and the at least one status bit to memory (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B).

11. Referring to claim 2, Nakayama has taught wherein the conditional jump instruction reads the digital value and the at least one status bit from memory to determine if the condition of the conditional jump instruction is satisfied (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B).

12. Referring to claim 3, Nakayama has taught wherein the at least one status bit is read from memory at the same time as the digital value (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B).

13. Referring to claim 4, Nakayama has taught wherein the memory has one or more addressable locations, and the at least one status bit is stored at the same addressable location as the corresponding digital value (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B). In regards to Nakayama, the sign bit is held at the same address location as the value.

14. Referring to claim 5, Nakayama has taught wherein the at least one status bit is set high if the digital value is zero (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B).

15. Referring to claim 6, Nakayama has taught wherein the at least one status bit is set high if the digital value is a positive value (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B). In regards to Nakayama, it does not matter whether the status bit is set high or low.

16. Referring to claim 7, Nakayama has taught wherein the at least one status bit is set high if the digital value is negative (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B). In regards to Nakayama, it does not matter whether the status bit is set high or low.

17. Referring to claim 8, Nakayama has taught wherein the at least one status bit is set high if the digital value is a non zero value (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B). In regards to Nakayama, it does not matter whether the status bit is set high or low.

18. Referring to claim 9, Nakayama has taught wherein the at least one status bit is set high based on the value of the least significant bit of the digital value (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B). In regards to Nakayama, it does not matter whether the status bit is set high or low.

19. Referring to claim 10, Nakayama has taught in a pipelined instruction processor that executes instructions including conditional jump instructions, one or more of the conditional jump instructions reading a digital value from memory to determine if the condition of the

conditional jump instruction is satisfied (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B), the improvement comprising:

a. Status bit generator for generating at least one status bit based on a digital value, the at least one status bit indicating if a predetermined condition of a conditional jump instruction is satisfied (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B); and

b. Storing means for storing the digital value and the at least one status bit to the memory (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B).

20. Referring to claim 11, Nakayama has taught wherein a selected conditional jump instruction reads the digital value and the at least one status bit from memory to determine if the condition of the conditional jump instruction is satisfied (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B).

21. Referring to claim 12, Nakayama has taught wherein the at least one status bit is read from the memory at the same time as the digital value is read (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B). In regards to Nakayama, it does not matter whether the status bit is set high or low.

22. Referring to claim 13, Nakayama has taught wherein the memory has one or more addressable locations, and the at least one status bit is stored at the same addressable location as the corresponding digital value (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2,

lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B). In regards to Nakayama, the sign bit is held at the same address location as the value.

23. Referring to claim 14, Nakayama has taught wherein the at least one status bit is set high if the digital value is zero (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B). In regards to Nakayama, it does not matter whether the status bit is set high or low.

24. Referring to claim 15, Nakayama has taught wherein the at least one status bit is set high if the digital value is a positive value (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B). In regards to Nakayama, it does not matter whether the status bit is set high or low.

25. Referring to claim 16, Nakayama has taught wherein the at least one status bit is set high if the digital value is negative (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B). In regards to Nakayama, it does not matter whether the status bit is set high or low.

26. Referring to claim 17, Nakayama has taught wherein the at least one status bit is set high if the digital value is anon zero value (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B). In regards to Nakayama, it does not matter whether the status bit is set high or low.

27. Referring to claim 18, Nakayama has taught wherein the at least one status bit is set high based on the value of the least significant bit of the digital value (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B). In regards to Nakayama, it does not matter whether the status bit is set high or low.

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claims 19-22 and 24-27 rejected under 35 U.S.C. 103(a) as being unpatentable over Watson et al., U.S. Patent Number 3,573,854 (herein referred to as Watson) in view of Nakayama et al., U.S. Patent Number 4,788,655 (herein referred to as Nakayama).

30. Referring to claim 19, Watson has taught in a pipelined instruction processor that executes instructions including conditional jump instructions, the improvement comprising:

a. A plurality of addressable registers, each of the addressable registers (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5);

b. Logic to access a current instruction (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5);

c. A jump look-ahead controller for generating a jump look-ahead signal using the address that identifies one of the addressable registers and the jump field that identifies a jump status bit within the identified addressable register, the jump look-ahead signal is a function of the identified jump status bit (Watson column 1,

lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5);

d. Tracking logic for tracking the addresses of a predetermined number of previous instructions in the pipelined instruction processor and comparing the addresses of each previous instruction to the address of the current instruction to generate a series of jump disable signals (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5); and

e. Conflict detection logic for generating a jump early signal using the jump look-ahead signal and the series of jump disable signals, the jump early signal initiates the conditional jump depending on the values of the jump disable signals (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

31. Watson has not taught:

a. One or more of the conditional jump instructions reading a digital value from memory to determine if the condition of the conditional jump instruction is satisfied;

b. Storing a value that includes a digital value and at least one jump status bit; and

c. Wherein the current instruction includes an address and a corresponding jump field, the address identifies one of the addressable registers and the corresponding jump field identifies a jump status bit of the at least one jump status bits within the identified addressable register.

32. Nakayama has taught:

a. One or more of the conditional jump instructions reading a digital value from memory to determine if the condition of the conditional jump instruction is satisfied (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B);

b. Storing a value that includes a digital value and at least one jump status bit (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B); and

c. Wherein the current instruction includes an address and a corresponding jump field, the address identifies one of the addressable registers and the corresponding jump field identifies a jump status bit of the at least one jump status bits within the identified addressable register (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B).

33. A person of ordinary skill in the art at the time the invention was made would have recognized that the condition code generating system of Watson requires less time to process and complete, thereby increasing the speed of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the condition code generating system to increase the speed of the processor.

34. Referring to claims 20 and 21, Watson has not taught

a. Wherein each jump status bit is dependent on the digital value stored in the corresponding addressable register; and

b. A bit status generator for generating the corresponding jump status bits.

35. Nakayama has taught:

a. Wherein each jump status bit is dependent on the digital value stored in the corresponding addressable register (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B); and

b. A bit status generator for generating the corresponding jump status bits (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B).

36. A person of ordinary skill in the art at the time the invention was made would have recognized that the condition code generating system of Watson requires less time to process and complete, thereby increasing the speed of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the condition code generating system to increase the speed of the processor.

37. Referring to claim 22, Watson has taught a prediction logic block responsive to the jump early signal for implementing a prediction algorithm to predict the conditional jump depending on the values of the jump disable signals (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

38. Referring to claim 24, Watson has taught wherein the predetermined number of instructions are sequentially piped through an execution pipeline after being piped through a pre-fetch pipeline, the execution pipeline includes a write-back stage (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

39. Referring to claim 25, Watson has taught wherein the addressable register is written during the write-back stage (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

40. Referring to claim 26, Watson has taught wherein the execution pipeline further includes an address generation stage, a present address stage, an output operand stage, a capture data stage, and an arithmetic operation stage, all before the write-back stage (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

41. Referring to claim 27, Watson has taught a method for determine if a condition of a conditional jump instruction is satisfied in a pipelined instruction processor, the method comprising:

a. Generating a jump look-ahead signal that is a function of the selected jump status bit read from the selected address location of the addressable memory, the identified jump status bit is accessed using the address and the jump field of the

current instruction (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5);

b. Tracking the addresses of a predetermined number of previous instructions in the pipelined instruction processor and comparing the addresses to the address of the current instruction to generate a series of jump disable signals (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5); and

c. Generating a jump early signal using the jump look-ahead signal and the series jump disable signals, the jump early signal initiates a conditional jump depending on the value of the jump disable signals (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

42. Watson has not taught:

a. Storing a digital value and one or more jump status bits that are based on the digital value in each of a plurality of address locations in an addressable memory; and

b. Accessing a current instruction, the current instruction having an address and a jump field, the address identifies a selected address location of the addressable

memory, and the jump field identifies a selected jump status bit of the selected address location.

43. Nakayama has taught:

a. Storing a digital value and one or more jump status bits that are based on the digital value in each of a plurality of address locations in an addressable memory (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B); and

b. Accessing a current instruction, the current instruction having an address and a jump field, the address identifies a selected address location of the addressable memory, and the jump field identifies a selected jump status bit of the selected address location (Nakayama Abstract; column 1, lines 9-13 and 49-68; column 2, lines 20-50; Figure 1A; Figure 1B; Figure 5A; and Figure 5B).

44. A person of ordinary skill in the art at the time the invention was made would have recognized that the condition code generating system of Watson requires less time to process and complete, thereby increasing the speed of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the condition code generating system to increase the speed of the processor.

45. Claim 23 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Watson in view of Nakayama as applied to claim 19 above, and further in view of Heuring and Jordan's Computer Systems Design and Architecture ©1997 (herein referred to as Heuring).

46. Watson in view of Nakayama has not taught wherein the tracking logic includes a queue for sequentially storing a pre-determined number of instructions prior to sequentially piping the

pre-determined number of instructions through a read stage and decode stage in a pre-fetch pipeline. Heuring has taught wherein the tracking logic includes a queue for sequentially storing a pre-determined number of instructions prior to sequentially piping the pre-determined number of instructions through a read stage and decode stage in a pre-fetch pipeline (Heuring Pages 92-95). A person of ordinary skill in the art at the time the invention was made would have recognized that pre-fetching increases the speed and efficiency of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the pre-fetching of Heuring to increase processor speed and efficiency.

Conclusion

47. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Zmyslowski et al., U.S. Patent Number 4,967,351, has taught a condition flag producing system.

b. Barbour et al., U.S. Patent Number 5,193,157, has taught a condition flag producing system.

c. Matsumoto et al., U.S. Patent Number 6,324,641, has taught a condition flag producing system.

48. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

49. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

50. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

October 20, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100